

Universal Battery Monitor Using the bq2018 Power Minder™ IC



Features

- Counts charge and discharge for Li-Ion, NiCd, NiMH, and other chemistries
- Works with host controller to form comprehensive battery pack monitor
- Direct connection to battery stack
- Connects to 4 to 12 series NiCd/NiMH cells or 2 to 4 Li-Ion series cells; other configurations available
- Low operating current
- Measures a wide dynamic range of current
- Small size
 - Entire circuit can fit on less than 0.5 square inches of PCB space
- Low implementation cost
 - Fewer than 15 discrete components required

Typical Applications

- Cellular telephones
- Personal digital assistants
- Other portable handheld equipment

Series 2018, Number One

Figure 1. bq2018 Circuit Connection





General Description

The circuit shown in Figure 3 is a typical bq2018 Power Minder implementation. The battery is connected between BAT+ and BAT-. Q1 and C5, in conjunction with the REG output, regulate the supply voltage to the bq2018 to between 3.5V and 3.9V for the varying battery input at BAT+. The SR V-to-F input pins sense the charge and discharge current using the low-value resistor R1.

A microcontroller communicates with the Power Minder IC using an I/O port connected to the bq2018 HDQ pin. The microcontroller reads the charge/discharge and timer counters of the bq2018 and calculates remaining battery capacity for communication to the user or to the system's power management controls. The bq2018 WAKE output pin alerts the microcontroller that charge/discharge activity greater than a programmable level is taking place.

The circuit monitors a battery pack of any chemistry. The typical operating parameters of the circuit are:

| Symbol | Parameter | Units |
|------------------------------|----------------------------|---------------|
| VI | Input voltage BAT+ to BAT- | 3.5V to 18.0V |
| I _{SR} | Measurable current range | ± 4A Max.(1) |
| I _{OPR} | Operating current | 80μΑ |
| I _S Sleep current | | 10μΑ |
| IBACK | Register backup current | < 0.1µA (2) |

(1) Assumes $50m\Omega$ 1W sense resistor and bq2018 offset compensation. (2) Provides years of backup time when using cell(s) from the battery stack.

Sense Resistor Selection

R1 must be sized properly to measure the entire range of charge and discharge currents in the application within the limits of the bq2018. The input parameters include:

- 1. The potential of the SR input is limited to -200mV to +200mV. The charge/discharge currents through the sense resistor must not produce a voltage greater than ±200mV.
- 2. The bq2018 counts charge and discharge at a rate of 12.5μ V per hour. Signals < 12.5μ V require greater than one hour to resolve. The designer should consider the resolution vs. time when selecting a sense resistor.

The sense resistor must also handle the power dissipation of all charge and discharge activity. The circuit example uses a $50m\Omega$ 1W sense resistor.

Measurement Offset

The bq2018 has a calibration test mode that measures the offset of the bq2018 based circuit. A final test setup for the battery pack can enable this mode by setting the appropriate bits in the bq2018. When the bq2018 is in calibration mode, no charge/discharge current should be applied. In calibration mode, the bq2018 measures the circuit offset and latches a value in the offset adjustment register. The host microcontroller uses the value in the register to periodically adjust the charge and discharge count values from the bq2018.

Note: Board layout affects offset. C2, C3, and C5 should be as close to the bq2018 as practical. Figure 2 shows one example of how to lay out the circuit in Figure 3.

Parts List

| ltem | Quantity | Reference | Part |
|------|----------|------------|--|
| 1 | 1 | U1 | bq2018 |
| 2 | 2 | R4, R6 | 1K |
| 3 | 1 | R5 | 100 |
| 4 | 2 | R3, R2 | 100K |
| 5 | 1 | C1 | 0.1μF/1.0μF |
| 6 | 3 | C4, C2, C3 | 0.1µF |
| 7 | 1 | C5 | 0.01µF/0.001µF |
| 8 | 1 | Q1 | SST108 |
| 9 | 1 | D3 | BAV99 |
| 10 | 1 | R1 | 0.05Ω tolerance = 2%, Watt = 1W |
| 11 | 2 | D2, D1 | BZX84C5V6 Zener |

Figure 2. bq2018 Circuit Board Layout



Microcode Example for HDQ Interface

| ;TITLE "HDQ.A ;LAST UPDATE: ;TIMING VALUES | ASM — 201XH 04/15/96 ARE FOR 8.0 | INTERFACE" MHz CRYSTAL | |
|--|---|--|---|
| RAM ASS | IGNMEN | Т | |
| W RTCC PC STATUS | EQU EQU EQU EQU | 00H 01H 02H 03H | ;PROGRAM COUNTER |
| X ; | EQU | 04H | ;FILE SELECT |
| ; PORTB ; | EQU | 06н | ;PORTB 0 is HDQ line |
| TIMEOUT HSERDAT HSERBIT WSTACK • | EQU EQU EQU EQU | 0AH 0BH 0CH 0DH | ;TIMEOUT FLAG, 0=NO TIMEOUT ;HIGH SERIAL DATA REGISTER ;HIGH SERIAL BIT COUNTER ;TEMP STORE FOR W REGISTER |
| HCMD | EQU | OFH | ;HOST COMMAND |
| , BTRIS | EQU | 1 FH | ;MIRROR TRISB |
| ORG | 00H | | |
| RESET | GOTO | BEGIN | |
| ; SUBROUT | INES | | |
| ; HIGH-SPEED SE | ERVICE FOR B | ATTERY | |
| ,HS_SERVA | MOVLW MOVWF | 08H HSERBIT | ;LOAD BIT COUNTER ;WITH 8 FOR 8 BITS |
| READIT CLRF | WSTACK | THEOLE | ;GET TIMEOUT READY |
| HABQR0 | BTFSS | PORTB, 0 | ;REQUEST FOR HS |
| | DECFSZ GOTO | WSTACK,1 HABQR0 | ;COUNT FOR TIMEOUT |
| ; ; TIME-OUT ON F | RECEIVE | - | |
| ; | MOVLW | OFFH | |
| | MOVWF GOTO | TIMEOUT BREAKIT | |
| ; HABQR1 RRF | HSERDAT,1 CLRF | WSTACK | ;SHIFT DATA ;TIME LOW TIME |
| HABQR2 | BTFSC GOTO INCF BTFSS GOTO | PORTB,0 HABQR3 WSTACK,1 WSTACK,6 HABQR2 | ;CHECK FOR STOP BIT ;BREAK DURING READ LOW 144us |
| ; ;break detected |) | | |
| ; BREAKIT | CLRF MOVLW MOVWF | HCMD 08H HSERBIT | ; CANCEL PENDING COMMAND ;LOAD BIT COUNTER ; WITH 8 FOR 8 BITS |
| HABQR5 | NOP BTFSS GOTO RETLW | PORTB,0 HABQR5 00H | ;CHECK FOR STOP BIT ;WILL LOOP FOREVER IF LINE STAYS LOW ;DONE |
| , HABQR3 | BSF MOVLW ANDWF BTFSS BCF DECFSZ | HSERDAT,7 30H WSTACK,W STATUS,2 HSERDAT,7 HSERDAT,1 | |
| ; | GOTO | READIT | ;MORE TO DO! |
| ; | MOVF | HSERDAT,W | |
| DONE_WA | MOVWF MOVLW MOVWF RETLW | HCMD 08H HSERBIT 00H | ;LOAD BIT COUNTER ; WITH 8 FOR 8 BITS |
| ; ; SNDA_IT WILL | SEND ONE BY | TE TO HDQ MODULE | |
| ; SNDA_IT | MOVLW MOVWF | 08H HSERBIT | ;LOAD BIT COUNTER ;WITH 8 FOR 8 BITS |
| ; ;DELAY A BIT | | | |
| ; | CLRF | HCMD | |

Microcode Example for HDQ Interface (continued)

| snda_1 | INCF BTFSS GOTO | HCMD,1 HCMD,6 SNDA 1 | |
|---------------------------------|---|---------------------------------------|---|
| ; snda_2 | BCF MOVF TRIS CLRF | BTRIS,0 BTRIS,W PORTB HCMD | |
| ; snda_3 | INCF BTFSS GOTO | HCMD,1 HCMD,4 SNDA_3 | |
| ; SNDA_5 | BTFSS GOTO | HSERDAT,0 SNDA_4 | ;TEST DATA BIT |
| ' | BSF MOVF TRIS | BTRIS,0 BTRIS,W PORTB | |
| ; snda_4 | CLRF | HCMD | |
| ; snda_7 | INCF BTFSS GOTO | HCMD,1 HCMD,5 SNDA_7 | |
| ; | BSF MOVF TRIS | BTRIS,0 BTRIS,W PORTB | |
| ; | CLRF BSF | HCMD HCMD,4 | |
| , snda_9 | INCF BTFSS GOTO | HCMD,1 HCMD,6 SNDA_9 | |
| | RRF DECFSZ GOTO | HSERDAT,1 HSERBIT,1 SNDA_2 | ;SHIFT DATA, FOR NEXT BIT ;DEC COUNTER ;MORE BITS TO SEND |
| , | CLRF MOVLW MOVWF RETLW | HCMD 08H HSERBIT 00H | ;LOAD BIT COUNTER ; WITH 8 FOR 8 BITS ;NO, DONE |
| ; ;INITIAI | JIZATI | o n | |
| ; BEGIN | CLRWDT MOVLW OPTION | 06н | |
| | CLRW MOVWF MOVLW MOVWF TRIS | PORTB 03H BTRIS PORTB | ;SET UP PORT |
| | MOVLW MOVWF | USH HSERBIT | ;LOAD BIT COUNTER ;WITH 8 FOR 8 BIT |
| OTHER USER COL | DE | | |
| ;READ EXAMPLE ; .READ DCR | | | |
| ; | MOVIW | 03H | |
| | MOVWF CALL CALL | HSERDAT SNDA_IT HS_SERVA | |
| ;; | HSERDAT=N. | AC | |
| ; ;WRITE EXAMPLE | 1 | | |
| ;WRITE RAM = C |)xAA | | |
| | MOVLW MOVWF | 83H HSERDAT | |
| | CALL MOVLW MOVWF CALL | SNDA_IT 0AAH HSERDAT SNDA IT | |
| ; | 011111 | _ | |
| ;OTHER USER C | CODE | - | |
| ;OTHER USER C ; | GOTO | _ RESET | |

Figure 3. bq2018 Schematic



C5—bypass for REG

R1—sense resistor

Interfacing to a Microcontroller

A microcontroller can interface the bq2018 using a general purpose I/O port. The WAKE output of the bq2018 interrupts the microcontroller when it detects charge or discharge activity greater than a programmable level. HDQ and WAKE are open-drain and require a pull-up resistor as shown.



Microcontroller Software

A microcontroller must configure the bq2018 and read and format its counter data to implement a battery capacity monitor. There are three main aspects of the software: Factory Configuration Program, Operating Program, and Serial Communication Program.

Factory Configuration Program (Test System Microcontroller)

The factory program configures a bq2018 based intelligent battery pack for operation. Actual battery monitor information, such as remaining capacity, compensation rates, and status flags may be stored in the bq2018 user RAM. The factory program initializes the user RAM and the bq2018. The battery maintains the bq2018 data with a low backup current of < 0.1μ A.



Note: 1. Write default values to RAM if necessary.

Operating Program (Host System Microcontroller)

The Operating program loop reads the bq2018 and updates the RAM locations for charge/discharge use conditions. The microcontroller periodically applies self-discharge and offset correction and calibrates remaining capacity and the full-charge reference based on state-of-charge and battery voltage.



Notes: 1. Requires A-to-D converter. 2. Typical loop time is once per minute.

Serial Communication Program (Test and Host Microcontroller)

The Designed to GO insert shows an example of the microcode required to communicate with the bq2018 using a port pin of a microcontroller. The code is for a PIC16C5X running at 8.0MHz.



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